



CASES 2002

CREST Center
Georgia Institute of technology
Atlanta, GA 30332-0205 USA

Non-Profit
Organization
U.S. POSTAGE
PAID
Atlanta, GA
Permit No. 4009

CASES 2002

International Conference on Compilers, Architecture, and Synthesis for Embedded Systems
October 8-11, 2002 • Grenoble, France

Advance Program

TUESDAY, OCTOBER 8, 2002

The conference will present two tutorials on October 8

Tutorial 1: Compilers for Embedded Processors: Technology and New Challenges

8:00-8:30 a.m. **Continental Breakfast**

10:30 a.m. **Break**

8:30 a.m. - 12 noon

Presenter: Rainer Leupers, Aachen University of Technology

Abstract: Programmable processors are among the major building blocks in today's embedded SoC designs. In contrast to desktop systems, there is a huge variety of domain specific and even application specific architectures, including microcontrollers, DSPs, NPUs, and ASIPs. The irregular architectures and very high code quality demands of embedded processors create a need for new compiler techniques beyond classical Dragon Book compilation. This tutorial gives an overview of today's retargetable compiler and code optimization technology for embedded processors, while also touching further important software development tools. Additionally, new research challenges in the areas of architecture exploration and compilation for recent architecture families like VLIWs and NPUs will be covered.

12:00 noon **Lunch (on your own see restaurant listing)**

Tutorial 2: Embedded system performance analysis

1:30 - 5:00 p.m. 3:30 p.m. **Break**

Presenters: Rolf Ernst, Technical University of Braunschweig Reinhard Wilhelm, University of Saarbrücken

Abstract: The trend in embedded system design is towards complex and heterogeneous systems-on-chip (SoC) which are often connected to larger, networked systems. An embedded system designer integrates IP components and subsystems including APIs using a similarly complex communication infrastructure. The resulting target architecture and its run-time system expose a complicated run-time behavior, which is hardly understood by any single person in the design team. The only current way to verify system performance is extensive simulation. Simulation corner case definition becomes increasingly difficult, leaving the designer with a growing design risk. Another problem is debugging.

In this tutorial, we will review target architecture modeling and performance analysis. Then, we will have a closer look at formal methods for system analysis as an alternative to simulation. Formal analysis has been used in real-time system design and we discuss techniques to apply some of the scheduling analysis methods to heterogeneous embedded system design. We will also present recent advances in formal process analysis including complicated cache architectures which found their way into commercial tools.

Hardware Accelerators

Mukud Sivaraman, Shail Aditya, Hewlett-Packard Labs, USA

An Adaptive CMP Architecture for Future Mobile Terminals

Mladen Nikitovic, Mats Brorsson Department of Microelectronics and Information Technology, Royal Institute of Technology (KTH), Sweden

Towards Automatic Synthesis of a Class of Application-Specific Sensor Networks

Amol Bakshi, Jingzhao Ou, Viktor K. Prasanna, Dept. of EE-Systems, University of Southern California, USA

11:00 a.m. **S3.2 Extensions and Benchmarks**

Hardware Implementation of the Ravenscar Ada Tasking Profile

Michael Ward and Neil C. Audsley
Department Computer Science, University of York, U.K.

Bit Section Instruction Set Extension of ARM for Embedded Applications

Bengu Li and Rajiv Gupta, Department of Computer Science, University of Arizona, USA

Code Coverage and Input Variability: Effects on Architecture and Compiler

Hillery C. Hunter and Wen-mei W. Hwu, University of Illinois at Urbana-Champaign, USA

12:30 p.m. **Lunch (on your own see restaurant listing)**

2:00 p.m. **Session 4 track S4.1 Power in Memory and Network Processors track S4.2 Program Transformations**

2:00 p.m. S4.1 Power in Memory and Network Processors An Integrated Approach to Reducing Power Dissipation in Memory Hierarchies

Jay Pisharath, Alok Choudhary, Department of Electrical and Computer Engineering, Northwestern University, USA

Embedded Cache Architecture with Programmable Write Buffer Support for Power and Performance Flexibility

Afzal Malik, Bill Moyer, Roger Zhou, Embedded Platform Solutions, Motorola Inc., USA

Increasing Power Efficiency of Multi-Core Network Processors through Data Filtering

Gokhan Memik, William H. Mangione-Smith, Department of Electrical Engineering, University of California, Los Angeles, USA

2:00 p.m. **S4.2 Program Transformations Cost Effective Memory Disambiguation for Multimedia Codes**

Esther Salami, Jesús Corbal, Carlos Álvarez and Mateo Valero, Departament d'Arquitectura de Computadors, Universitat

PACT HDL: A C Compiler Targeting ASICs and FPGAs with Power and Performance Optimizations

Alex Jones, Debabrata Bagchi, Satrajit Pal, Xiaoyong Tang, Alok Choudhary, Prith Banerjee, Center for Parallel and Distributed Computing, Technological Institute, Northwestern University, USA

6:00 p.m. **Banquet**

FRIDAY OCTOBER 11, 2002

8:00-8:30 a.m. **Continental Breakfast**

8:30 a.m. **Session 7 Embedded System Techniques (2)**

Wave Pipelining for Application-Specific Networks-on-Chips

Jiang Xu, Wayne Wolf, Department of Electrical Engineering, Princeton University, USA

Handling of Packet Dependencies: A Critical Issue for Highly Parallel Network Processors

Stephen Melvin, FlowStorm, Inc., USA, Yale Patt, University of Texas, USA

On Achieving Balanced Power Consumption in Software Pipelined Loops

Hongbo Yang, Guang R. Gao, Clement Leung, University of Delaware, USA

Low Power Control Techniques for TFT LCD Displays

Franco Gatti, Andrea Acquaviva, Luca Benini, Bruno Ricco, DEIS - University of Bologna, Italy

10:30 a.m. **Break**

11:00 a.m. **Session 8 track S8.1 Power and Battery Management track S8.2 System Synthesis**

11:00 a.m. **S8.1 Power and Battery Management**

Dynamic Battery State Aware Approaches for Improving Battery Utilization

Sung I. Park, Mani B. Srivastava, Networked and Embedded Systems Laboratory, Electrical Engineering Departments, University of California, Los Angeles, USA

System Lifetime extension by battery management: an experimental work

Davide Brui, Luca Benini, Bruno Riccò, D.E.I.S., University of Bologna, Italy

Process Cruise Control - Event-Driven Clock Scaling for Dynamic Power Management

Andreas Weissel, Frank Bellosa, University of Erlangen, Germany

11:00 a.m. **S8.2 System Synthesis**

HW / SW partitioning approach for reconfigurable system

WEDNESDAY, OCTOBER 9, 2002

12:30 p.m. **Welcome Lunch (provided)**
2:00-3:30 p.m. **Keynote 1: Giovanni De Micheli** Stanford University, Joint Talk CASES'02/EMSOFT'02
Keynote 2: John Rayfield ARM Ltd., Joint Talk CASES'02/EMSOFT'02

3:30-4:00 p.m. **Break**

4:00-5:30 p.m. **Invited Talks**
Physical Programming: Beyond Mere Logic
Bran Selic, Rationale
Processes, Interfaces and Platforms. Embedded Software Modeling in Metropolis
Luciano Lavagno, Politecnico di Torino and Cadence Labs
Compiling with Code-Size Constraints
Jens Palsberg, Purdue University

THURSDAY OCTOBER 10, 2002

8:00-8:30 a.m. **Continental Breakfast**
8:30-10:30 a.m. **Session 2 Embedded System Techniques (1)**
A Case for Dynamic Pipeline Scaling
Jinson Koppanalil, Prakash Ramrakhiani, Sameer Desai, Anu Vaidyanathan, Eric Rotenberg, Dept of Electrical and Computer Engineering, North Carolina State University, USA
A Near-Optimal Instruction Scheduler for A Tightly Constrained, Variable Instruction Set Embedded Processor
Jack Liu, Fred Chow, Cognigine Corporation, USA
Components for Embedded Software - The PECOS approach
Thomas Genssler, Forschungszentrum Informatik (FZI), Germany, Oscar Nierstrasz, Software Composition Group S (CG), University of Bern, Switzerland Bastiaan Schoenhage, Object Technology International (OTI), The Netherlands
Efficient Architecture/Compiler Co-Exploration for ASIPs
Dirk Fischer, Jürgen Teich, Michael Thies, Ralph Weper, University of Paderborn, Germany

10:30 a.m. **Break**

11:00 a.m. **Session 3**
track S3.1 Architecture Adaptation and Synthesis
track S3.2 Extensions and Benchmarks
11:00 a.m. **S3.1 Architecture Adaptation and Synthesis**
Cycle-time Aware Architecture Synthesis of Custom

Politècnica de Catalunya, Spain
Optimizing Inter-Nest Data Locality
M. Kandemir, I. Kadayif, Microsystems Design Lab, Pennsylvania State University, USA, A. Choudhary, J. A. Zambreno, ECE Department, Northwestern University, USA
Leakage-Proof Program Partitioning
Tao Zhang, Santosh Pande, Andre dos Santos, Georgia Institute of Technology, College of Computing, USA, Franz Josef Bruecklmayr, Infineon Technologies, Germany

3:30 p.m. **Break**

4:00 p.m. **Session 5 Panel Embedded Architectures: Configurable, Re-configurable, ...or What?**

5:00 p.m. **Session 6 track S6.1 Scheduling and Frequency Scaling for Power track S6.2 Compilers and Program Analysis**

5:00 p.m. **S6.1 Scheduling and Frequency Scaling for Power Dynamic Voltage Leveling Scheduling for Real-Time Embedded Systems on Low-Power Variable Speed Processors**

Jian-Liang Kuo and Tien-Fu Chen, Department of Computer Science, National Chung Cheng University, Taiwan

Control-Theoretic Dynamic Frequency and Voltage Scaling for Multimedia Workloads

Zhijian Lu, Jason Hein, Mircea Stan, John Lach, Dept. of Electrical and Computer Engineering, University of Virginia, USA, Kevin Skadron, Marty Humphrey, Department of Computer Science, University of Virginia, USA

Energy Aware Task Scheduling with Task Synchronization for Embedded Real Time Systems

Ravindra Jejurikar and Rajesh Gupta, Center for Embedded Computer Systems, Department of Information and Computer Science, University of California at Irvine, USA

5:00 p.m. **S6.2 Compilers and Program Analysis**

Scenario-Based Software Characterization as a Contingency to Traditional Program Profiling

Jeffrey T Russell, Margarida F Jacome, University of Texas at Austin, Department ECE, USA

Experience with a Retargetable Compiler for a Commercial Network Processor

Jinhwan Kim, Sungjoon Jung, Yunheung Park, Electrical Engineering & Computer Science Department, Korea Advanced Institute of Science & Technology, Korea, Gang-Ryung Uh, Agere Systems, USA

des gn

K. Ben Chehida ad M. Auguin, I3S, University of Nice Sophia Antipolis, France

An Efficient Technique for Exploring Register File Size in ASIP Synthesis

Manoj Kumar Jain, M. Balakrishnan, Anshul Kumar IIT, India
Instruction Generation and Regularity Extraction For Reconfigurable Processors

Philip Brisk, Adam Kaplan, Ryan Kastner, Majid Sarrafzadeh Computer Science Department, University of California, Los Angeles, USA

12:30 p.m. **Lunch (on your own see restaurant listing)**

2:00 p.m. **Session 9 track S9.1 Software Transformation track S9.2 Embedded Programs**

2:00 p.m. **S9.1 Software Transformation**

Automatic Floating-point to Fixed-point Conversion for DSP Code Generation

Daniel Menard, Daniel Chillet, INRIA, LASTI – University of Rennes 1, France, François Charot, Olivier Sentieys, INRIA, IRISA, France
Iterative Procedural Abstraction for Code Size Reduction
Dae-Hwan Kim, Hyuk Jae Lee, School of Electrical Engineering and Computer Science, Seoul National University, Korea

Validating Software Pipelining Optimizations
Raya Leviathan, Amir Pnueli, Department of Computer Science, Weizmann Institute of Science, Israel

2:00 p.m. **S9.2 Embedded Programs**

Ensuring Code Safety Without Runtime Checks for Real-Time Control Systems

Sumant Kowshik, Dinakar Dhurjati, Vikram Adve, University of Illinois at Urbana-Champaign, USA

Predictable Programs in Barcodes

Alwyn Goodloe, Michael McDougall, Carl A. Gunter, Rajeev Alur Department of Computer and Information Science, University of Pennsylvania, USA

Real Java for Real Time - Gain and Pain

Anders Nilsson, Torbjörn Ekman, Klas Nilsson, Department of Computer Science, Lund University, Sweden

Program Concludes

Cutoff for On-Line Registration: October 3, 2002
On-Site Registration available
Cutoff for Conference Price Hotel Registration: September 1, 2002
For more information visit our web site at www.crest.gatech.edu/conferences/cases2002

General Co-Chairs

Shuvra S. Bhattacharyya, *University of Maryland*
Trevor Mudge, *University of Michigan*

Program Co-Chairs

Wayne Wolf, *Princeton University*
Ahmed Jerraya, *TIMA, Grenoble, France*

Steering Committee

Guang R. Gao, *University of Delaware*
Vinod Kathail, *Hewlett-Packard Labs*
Edward Lee, *University of California Berkeley*
Jaime Moreno, *IBM T.J. Watson Research Center*
Krishna V. Palem, *Georgia Institute of Technology*
Wayne Wolf, *Princeton University*

Co-Ordination Vice-Chair

Bruce Jacob, *University of Maryland*

Tutorial Chairs

X. Sharon Hu, *University of Notre Dame*
Joerg Henkel, *NEC*

Publications Vice-Chair

Jack Davidson, *University of Virginia*

Publicity Vice-Chair

Frank Mueller, *North Carolina State University*

Electronic Review Chair

Sungjoo Yoo, *TIMA Laboratory, France*

Representatives

Luciano Lavagno
University of Udine/Cadence, Italy (for Europe)
Hiroto Yasuura
Kyushu University, Japan (for Asia)

Local Arrangements Vice-Chair

Ahmed Jerraya, *TIMA, Grenoble, France*

REGISTRATION FORM

GIT-182 CASES 2002 (x35-509) October 8-11, 2002 Grenoble, France

Conference Fee: \$375 early \$450 late (cut off date: September 17, 2002)

Tutorial 1: \$150

Tutorial 2: \$150

Student Fee: \$225 early \$275 late (cut off date: September 17, 2002)

Tutorial 1 and 2: \$200

Please send my confirmation via e-mail.

I cannot attend this program, but add me to your mailing list.

PLEASE PRINT CLEARLY

Name: _____

*Social Security #: _____

Position: _____

Organization: _____

Address: _____

(The confirmation will be sent to this address, unless requested by e-mail.)

City: _____

State: _____ ZIP: _____

Daytime phone #: _____

FAX #: _____

E-mail: _____

Yes, I am a Georgia Tech graduate!

Amount Enclosed \$ _____

Check enclosed (payable to Georgia Tech)

Please include attendee's name, course number, and course date on all checks.

Charge: o American Express VISA MasterCard Discover

Card #: _____

Exp. Date: _____

Cardholder's Name: _____

Signature: _____

How did you hear about the course?

brochure web e-mail fax radio magazine ad

co-worker other _____

* Security number is required for Life Long Learning Tax Credits.

FEI # 58-6002023

SPONSORS

